

G703/64A

User Manual

 **Megatel Industries Corp.**

6 Crimson Drive
Norristown, PA 19401, USA
TEL: 610-239-8812 FAX: 610-239-8395
[Http://www.megatelindustries.com](http://www.megatelindustries.com)
info@megatelindustries.com

G703/64A I/F Converter

Description

The **G703/64A** interface converter allows full conversion between G.703 codirectional, contradirectional or centradirectional 64Kbps interfaces and CCITT V.35, X.21, RS-449 and EIA RS232 hardware. The interface converters are very easy to implement. Simply connect the appropriate interface cables, connect the external DC power adapter, and select the required “Direction” and “Timing” for translation. This product family features full compliance with all the relevant CCITT & EIA standards under 64Kbps network environments, with high reliability.

This product may be used widely in the Packet Switching Network, ISDN and DDN. It is also useful for data terminals to access PCM, 64K/2048Kbps digital channels as well as digital microwave channels. Additionally, it may be connected to Satellite Communication Channels such as SPAR series.

The typical application in this regard is indicated in the following figure.

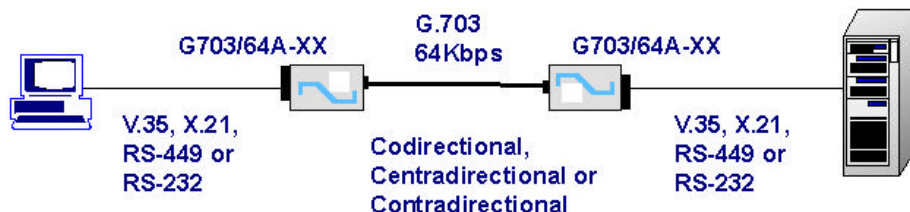


Figure 1; G703/64A Point-to-Point Application

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G.703 Interface

The G.703 Interface used in the **G703/64A** has a through rate of 64Kbps and is configurable in any one of three modes as described in more detail below.

Codirectional

The term codirectional is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (see Figure 2).

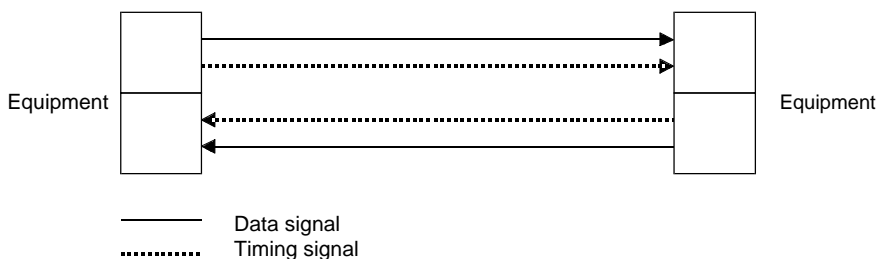


Figure 2; Codirectional interface

This mode is the most popular for point-to-point applications. In this case, both **G703/64A** units should have their *Direction* switch set to the “CO” or codirectional mode. All timing modes (recovery, transparent, dataport or oscillator) are possible in this mode.

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G.703 Codirectional Code Conversion Rules

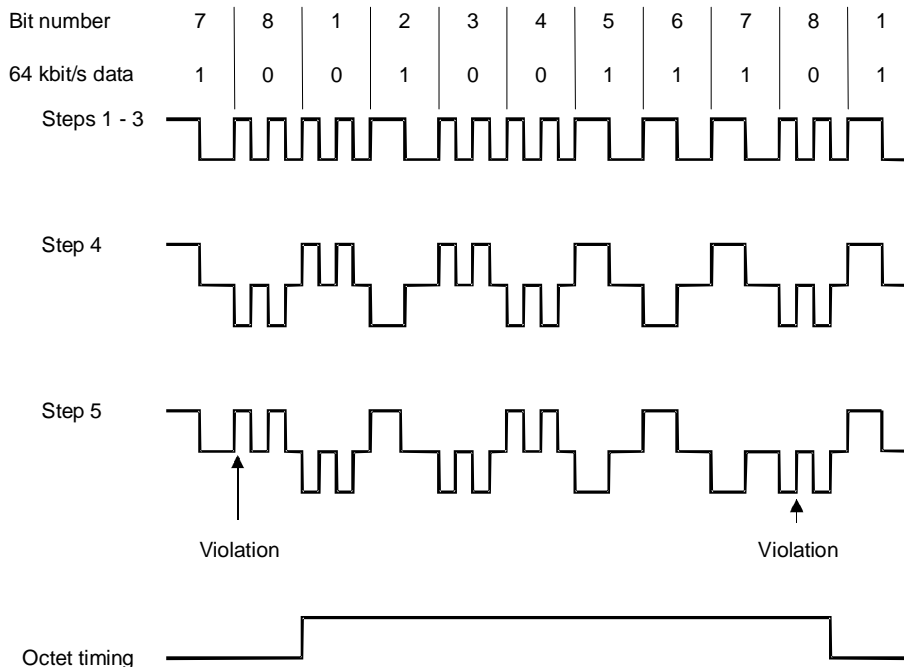
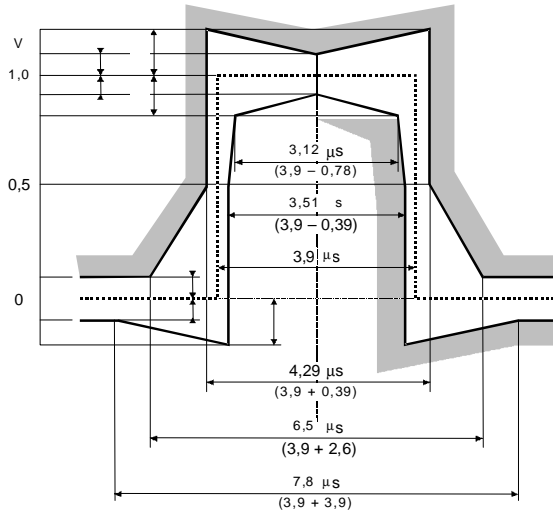


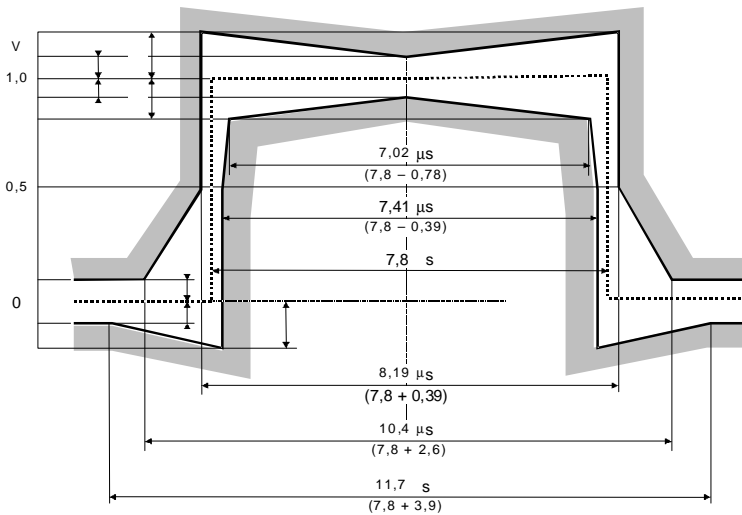
Figure 3; G.703 Codirectional Code Conversion Rules Illustration

- Step 1: A 64Kbps period is divided into four unit intervals.
- Step 2: A binary “one” is coded as a block of four bits “1100”.
- Step 3: A binary “zero” is coded as a block of four bits “1010”.
- Step 4: The binary signal is converted into a three-level signal.
- Step 5: A “Violation” block marks the last bit in an octet.

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a) Mask for *single pulse*



b) Mask for *double pulse*

Figure 4; Pulse Masks for the 64Kbps codirectional interface.

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Centradirectional

The term centradirectional (centralized clock) is used to describe an interface wherein for both directions of transmission of the information signal and the associated timing signals, a centralized clock (see Figure 5) is supplied.

Note – The codirectional and centradirectional interfaces should be used for synchronized networks and for plesiochronous networks having clocks of the stability required to ensure an adequate interval between the occurrence of slips.

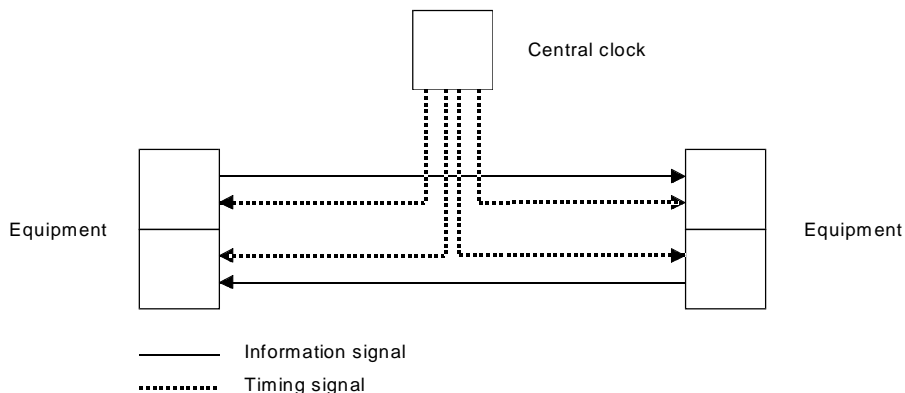


Figure 5; Centradirectional (centralized clock)

In this mode, both **G703/64A** units must have their *Direction* switch set to “CENTRA” for centradirectional. The *Timing* in this application may only be set to “RECOVERY” on both units.

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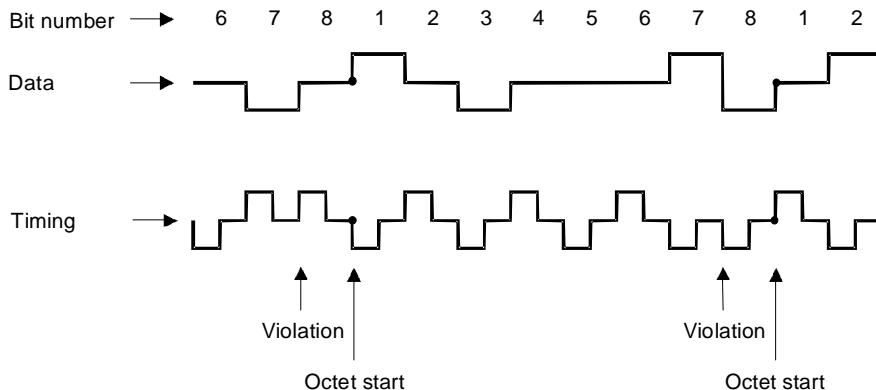


Figure 6; Signal structure of central clock interface.

The drawing above shows the structure of the signals and their nominal phase relationships. The data signals are coded in AMI code. The composite timing signals convey the 64KHz bit-timing information using AMI code and 8KHz octet-phase information by introducing violations of the code rule.

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Contradirectional

The term contradirectional is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (see Figure 7).

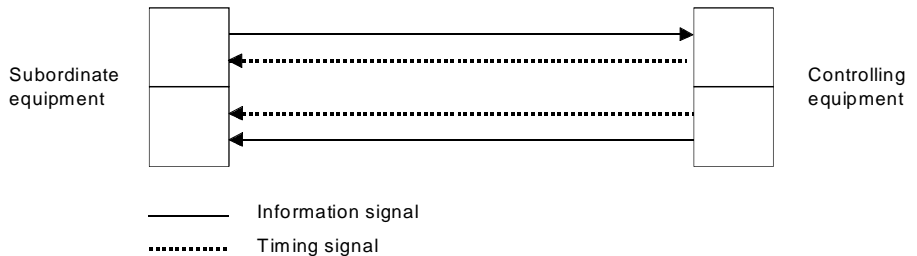


Figure 7; Contradirectional interface

In the above configuration, the controlling unit should have its *Direction* switch set to “CONTRA” for contradirectional code. The subordinate unit should be set to “CENTRA” as its timing signals are derived externally from the controlling unit. The *Timing* source for the controlling unit may be derived from the “Internal” oscillator or from the ETC on the “Dataport”. The *Timing* source on the subordinate unit may be set to the “RECOVERY” position only.

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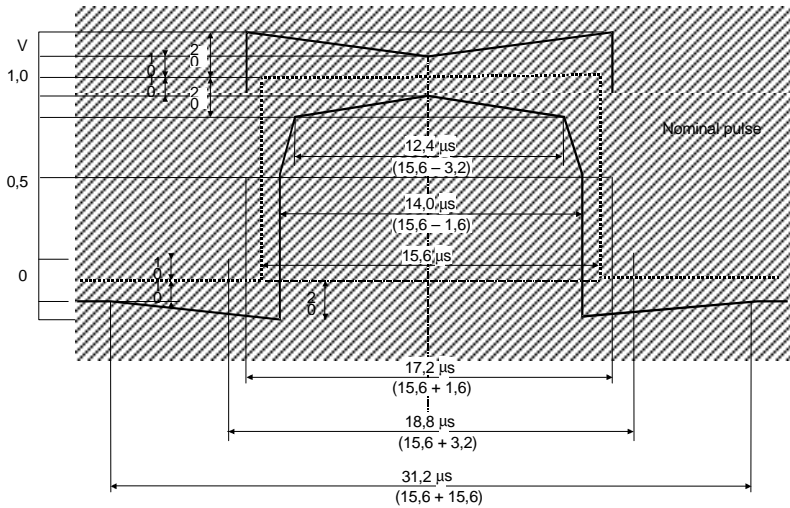


Figure 8; Mask of data pulse for contra/centradirectional I/F.

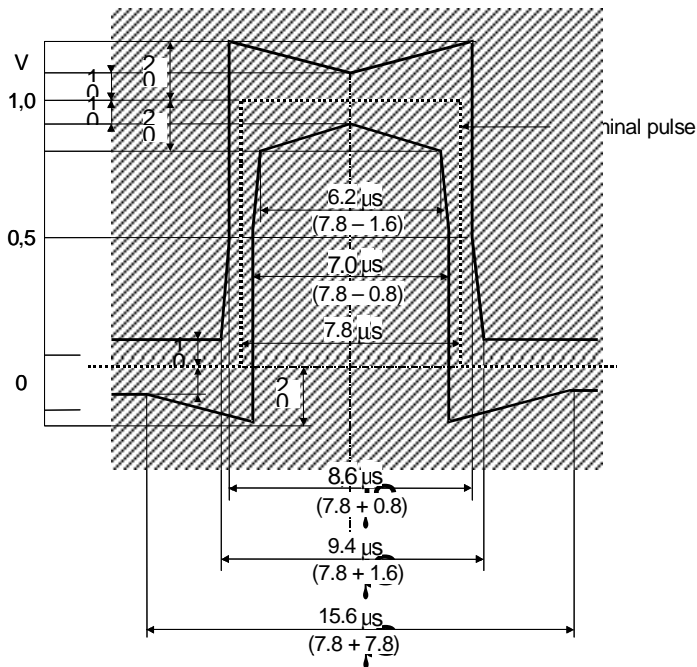


Figure 9; Mask of timing pulse for contra/centradirectional I/F.

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DATAPORT INTERFACE

The Data Port interface of the **G703/64A** is available in two different electrical configurations. Configuration #1 is RS-530 standard (balanced) on a DB25F connector, from which V.35, X.21 and RS-449 are derived via adapter cables. Configuration #2 is RS-232 (V.24) standard (unbalanced) on a DB25F connector, from which RS-232 (SYNC or ASYNC) is derived directly. The actual DB25F pin connector definitions and adapter cable pinouts may be found in the Appendix of this manual.

Features

- ◆ Single port access to 64Kbps services.
- ◆ Interface conversion between G.703 and V.35, X.21, RS449 or RS232.
- ◆ Data rate: 64Kbps for Synchronous mode.
19.2Kbps for Asynchronous mode.
- ◆ Fully transparent signal conversion.
- ◆ Adapter cable DCE/DTE switchable.
- ◆ DC +9V input power.

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Specifications

CCITT G.703 Interface Specifications :

◆TYPE	Co/Contra/Centradirectional 64Kbps.
◆Line	4 wires, 0.5 -0.7mm twisted pair cable.
◆Range	Up to 800m over 24AWG cable or better.
◆Impedance	120Ω.
◆"Pulse" amplitude	1.0V Nominal ± 10%.
◆"Zero" amplitude	0V Nominal ± 0.1V.
◆Clock frequency	64Kbps.
◆Frequency tracking	± 100ppm.
◆Interface connector	RJ45.
◆Complies with	CCITT G.703 and G.823.
◆Frame format	Unframe only.
◆Line code	64Kbps co/centra/contradirectional line code.

Data Communications Interface Specifications :

◆Interface Type	RS232; DB25-DB25 1-to-1 cable. RS530; DB25-DB25 1-to-1 cable. V.35; MB34-DB25 adapter cable. X.21; DB15-DB25 adapter cable. RS449; DB37-DB25 adapter cable.
◆Data rate	64Kbps for synchronous. 19.2Kbps for Asynchronous.
◆Connector	DB25/F.
◆Data type	Balanced for V.35, X.21, and RS449. Unbalanced for RS232.

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Indicators

◆ Signal Loss	G.703 Signal loss.
◆ Timing Loss	G.703 Timing loss.
◆ RD	Receive data.
◆ SD	Send data.
◆ POWER	DC9V input power.
◆ GRD	G.703 Receive data.
◆ GSD	G.703 Transmit data.

OPERATION: Front Panel SWITCH Functions

Loopback

Dataport	Digital loopback testing enabled at the data port.
Normal	Normal operational mode.
Analog	Analog loopback testing enabled at the G.703 side.

Direction

Centra	G.703 64Kbps Centradirectional type
Contra	G.703 64Kbps Contradirectional type
Co	G.703 64Kbps Codirectional type

Timing

Recovery	Timing is recovered from the G.703 side.
X parent	Transparent timing is employed.
Dataport	Timing is from the data side ETC clock.
OSC	Timing is from the internal oscillator clock.

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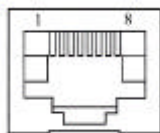
Notes:

Appendix

Pin Assignment:

The data port side of the **G703/64A** employs a DB25F connector. The interface circuitry is hardwired for either RS232 (unbalanced) or RS530 (balanced) on the circuit board, depending on the model ordered. The appropriate interface cable is supplied to adapt to the proper external connector. The following reference tables show the pin assignments for the G.703 interface and the data port interfaces RS232, X.21, V.35, RS530 and RS449. Note that for the balanced interface models, the dataport connector on the **G703/64A** is RS530 standard, while for the unbalanced model, the dataport is RS232 standard.

G.703 port pin assignment			
RJ-45 Pin No.	Pin Name	Direction of Signal	Command
1	Contradirectional timing	Output	
2	Contradirectional timing	Output	
3	Transmit data	Output	
4	Receive data	Input	
5	Receive data	Input	
6	Transmit data	Output	
7	Centradirectional timing	Input	
8	Centradirectional timing	Input	



RJ-45 Socket

Appendix

RS-232 pin assignment				
Signal Function	DB25 Pin No.	EIA Circuit	Direction of Signal	Command
Shield	1	AA	-----	
Ground	7	AB	-----	
TD	2	BA	Input	
RD	3	BB	Output	
RTS	4	CA	Input	Note 1
CTS	5	CB	Output	Note 1
DSR	6	CC	Output	Note 2
DCD	8	CF	Output	
TC	15	DB	Output	
RC	17	DD	Output	
DTR	20	CD	Input	Note 2
ETC	24	DA	Input	

Note 1: RTS and CTS internally connected together.

Note 2: DSR and DTR internally connected together.

X.21 pin assignment					
Signal Function	DB25 Pin No.	DB15 Pin No.	Circuit Name	Direction of Signal	Command
Shield	1	1	Shield	-----	
Ground	7	8	Ground	-----	
TD(A)	2	2	Transmit	Input	
TD(B)	14	9			
RD(A)	3	4	Receive	Output	
RD(B)	16	11			
RTS(A)	4	3	Control	Input	
RTS(B)	19	10			
DCD(A)	8	5	Indication	Output	
DCD(B)	10	12			
RC(A)	17	6	Signal Timing	Output	
RC(B)	9	13			

Appendix

V.35 pin assignment				
Signal Function	DB25 Pin No.	DB34 Pin No.	Direction of Signal	Command
Shield	1	A	-----	
Ground	7	B	-----	
TD(A)	2	P	Input	
TD(B)	14	S		
RD(A)	3	R	Output	
RD(B)	16	T		
RTS	4	C	Input	Note 1
CTS	5	D	Output	Note 1
DSR	6	E	Output	Note 2
DTR	20	H	Input	Note 2
DCD	8	F	Output	
TC(A)	15	Y	Output	
TC(B)	12	AA		
RC(A)	17	V	Output	
RC(B)	9	X		
ETC(A)	24	U	Input	
ETC(B)	11	W		

Note 1: RTS and CTS internally connected together.

Note 2: DSR and DTR internally connected together.

Appendix

RS-530 pin assignment				
Signal Function	DB25 Pin No.	Circuit	Direction of Signal	Command
Shield	1	AA	-----	
Ground	7	AB	-----	
TD(A)	2	BA	Input	
TD(B)	14			
RD(A)	3	BB	Output	
RD(B)	16			
RTS(A)	4	CA	Input	Note 1
RTS(B)	19			
CTS(A)	5	CB	Output	Note 1
CTS(B)	13			
DSR(A)	6	CC	Output	Note 2
DSR(B)	22			
DTR(A)	20	CD	Input	Note 2
DTR(B)	23			
DCD(A)	8	CF	Output	
DCD(B)	10			
TC(A)	15	DB	Output	
TC(B)	12			
RC(A)	17	DD	Output	
RC(B)	9			
ETC(A)	24	DA	Input	
ETC(B)	11			

Note 1: RTS(A) and CTS(A), RTS(B) and CTS(B) internally connected together.

Note 2: DSR(A) and DTR(A), DSR(B) and DTR(B) internally connected together.

Appendix

RS-449 pin assignment					
Signal Function	DB25 Pin No.	DB37 Pin No.	Circuit	Direction of Signal	Command
Shield	1	1		-----	
Ground	7	19,20,37	SG,RC,SC	-----	
TD(A)	2	4	SD	Input	
TD(B)	14	22			
RD(A)	3	6	RD	Output	
RD(B)	16	24			
RTS(A)	4	7	RS	Input	Note 1
RTS(B)	19	25			
CTS(A)	5	9	CS	Output	Note 1
CTS(B)	13	27			
DSR(A)	6	11	DM	Output	Note 2
DSR(B)	22	29			
DTR(A)	20	12	TR	Input	Note 2
DTR(B)	23	30			
DCD(A)	8	13	RR	Output	
DCD(B)	10	31			
TC(A)	15	5	ST	Output	
TC(B)	12	23			
RC(A)	17	8	RT	Output	
RC(B)	9	26			
ETC(A)	24	17	TT	Input	
ETC(B)	11	35			

Note 1: RTS(A) and CTS(A), RTS(B) and CTS(B) internally connected together.

Note 2: DSR(A) and DTR(A), DSR(B) and DTR(B) internally connected together.